LSI DOCKET NO. 01-849

CLAIMS:

What is claimed is:

1. A data transfer apparatus for transferring data from a first clock domain to a second clock domain, the data transfer apparatus comprising:

a first bank of registers having an input and an output, wherein the input receives a first size of data and the output outputs a second size of data in which the second size of data is twice the first size of data;

a second bank of registers having an input and an output, wherein the input receives a first size of data and the output outputs a second size of data in which the second size is twice the first size; and

a switch having a first input connected to the output of the first bank of registers, a second input connected to the output of the second bank of registers and an output, wherein the switch selects data from one of the first bank of registers and a second bank of registers for output at the output to the second clock domain,

wherein filling of data and transferring of data occurs in an alternating fashion between the first bank of registers and the second bank of registers such that one bank of registers is filled with data while another bank of registers transfers data to a synchronizer unit.

2. The data transfer apparatus of claim 1, wherein data is transferred from the output of the switch to the second clock domain through a synchronizer unit connected to the output of the switch, wherein the synchronizer unit synchronizes a transfer of data of the second size from one of the first bank of registers or the second bank of registers selected by the switch to the second clock domain.

3. The data transfer apparatus of claim 1, wherein the switch is a multiplexer.

4. The data transfer apparatus of claim 1, wherein the first bank of registers stack data of the first size to form data of the second size.

5. The data transfer apparatus of claim 1, wherein the first bank of registers comprises:

a first multiplexer having a first input input, a second input, and an output, wherein data of the first size is received at the second input from a data source;

a first latch having an input and an output, wherein the input is connected to the output of the first multiplexer and the output is connected to the first input of the first multiplexer;

a second multiplexer having a first input input, a second input, and an output, wherein data of the first size is received at the second input from the source; and

a second latch having an input and an output, wherein the input is connected to the output of the second multiplexer and the output is connected to the first input of the second multiplexer,

wherein the output of the first latch and the output of the second latch form the output of the second bank of registers and wherein the first multiplexer and the second multiplexer are alternately enabled to receive data from the source.

6. The data transfer apparatus of claim 3, wherein the second bank of registers comprises:

a third multiplexer having a first input input, a second input, and an output, wherein data of the first size is received at the second input from a data source;

a third latch having an input and an output, wherein the input is connected to the output of the third multiplexer and the output is connected to the first input of the third multiplexer;

a fourth multiplexer having a first input input, a second input, and an output, wherein data of the first size is received at the second input from the source; and

a fourth latch having an input and an output, wherein the input is connected to the output of the fourth multiplexer and the output is connected to the first input of the fourth multiplexer,

wherein the output of the first latch and the output of the fourth latch form the output of the second bank of registers and wherein the third multiplexer and the fourth multiplexer are alternately enabled to receive data from the source.

7. The data transfer apparatus of claim 1 further comprising:

at least one more bank of registers having an input and an output, wherein the input receives a first size of data and the output outputs a second size of data in which the second size

is twice the first size, wherein the switch includes a third input connected to the output of the third bank of registers and wherein filling of data and transferring of data in the first bank of registers, the second bank of registers, and the at least one more bank of registers rotates between the first bank of registers, the second bank of registers, and the at least one more bank of registers to avoid corruption of data transferred to the second clock domain.

8. The data transfer apparatus of claim 1, wherein the first size of data is 16 bits and the second size of data is 32 bits.

9. The data transfer apparatus of claim 1, wherein the first size of data is 32 bits and the second size of data is 64 bits.

10. The data transfer apparatus of claim 1, wherein the first clock domain is slower than the second clock domain.

11. A method for data transfer between a slower clock domain having a first bandwidth and a faster clock domain having a second bandwidth in which the first bandwidth is smaller than the second bandwidth in which data is transferred on every clock cycle in the slower clock domain, the method comprising:

stacking data into one group for transfer, wherein the one group has a size up to the second bandwidth;

stacking additional data into another group while transferring the one group to the second clock domain, wherein the another group has the size of the one group; and

repeating the stacking steps until data transfer is complete.

12. The method of claim 11, wherein the first bandwidth is 16 bits and the second bandwidth is 32 bits.

13. The method of claim 11, wherein the stacking steps are performed using a data capture unit.

14. The method of claim 11, wherein the data capture unit includes a set of registers.

15. The method of claim 11, wherein the data is passed to the second clock domain using a synchronizer circuit.

16. The method of claim 11, wherein the first bandwidth is 16 bits and the second bandwidth is 48 bits.

17. An apparatus for data transfer between a slower clock domain having a first bandwidth and a faster clock domain having a second bandwidth in which the first bandwidth is smaller than the second bandwidth in which data is transferred on every clock cycle in the slower clock domain, the apparatus comprising:

first stacking means for stacking data into one group for transfer, wherein the one group has a size up to the second bandwidth;

second stacking means for stacking additional data into another group while transferring the one group to the second clock domain, wherein the another group has the size of the one group; and

repeating means for repeating initiation of the first stacking means and the second stacking means until data transfer is complete.

18. The apparatus of claim 17, wherein the first bandwidth is 16 bits and the second bandwidth is 32 bits.

19. The apparatus of claim 17, wherein the stacking means are located in a data capture unit.

20. The apparatus of claim 17, wherein the data capture unit includes a set of registers.

21. The apparatus of claim 17, wherein the data is passed to the second clock domain using a synchronizer circuit.

22. The apparatus of claim 17, wherein the first bandwidth is 16 bits and the second bandwidth is 48 bits.